WHAT IS CLAIMED IS:

1. A circuit, comprising:

a volatile memory array;

a logic circuit operable to detect a memory array tamper situation and generate at least one control signal responsive thereto; and

circuitry associated with each of a plurality of individual cells within the volatile memory array which responds to the at least one control signal and by destroying any data stored by the associated memory cell.

2. The circuit of claim 1 wherein the circuit comprises a smart card.

3. The circuit of claim 1 wherein the individual cells comprise 6T type cells.

4. The circuit of claim 1 wherein each individual cell comprises a data latch, and the circuitry destroys the data stored by the data latch in response to the at least one control signal.

5. The circuit of claim 1 wherein the data latch includes a latch node and the circuitry drives the latch node to a reference voltage.

6. The circuit of claim 1 wherein each individual cell is connected to a bit line and the circuitry drives the bit line to a reference voltage.

7. The circuit of claim 1 wherein each individual cell comprises a data latch, and the circuitry unbalances the latch in response to the at least one control signal to destroy the data stored therein.

8. The circuit of claim 1 wherein each individual cell comprises a data latch having a first and a second side, and the circuitry exercises unique reference voltage control over each side of the latch in response to the at least one control signal to destroy the data stored therein..

9. A memory circuit, comprising:

a data latch having a true node and a complement node; and

circuitry responsive to a control signal to short the true node to the complement node for the purpose of destroying data stored by the latch.

10. The circuit of claim 9 wherein the circuitry comprises a p-channel transistor having its conduction terminals connected between the true node and the complement node and its gate connected to receive the control signal.

11. The circuit of claim 9 wherein the circuitry comprises an n-channel transistor having its conduction terminals connected between the true node and the complement node and its gate connected to receive the control signal.

12. The circuit of claim 9 wherein the memory circuit further includes:

a first pass gate coupling the true node to a bit line;

a second pass gate coupling the complement node to a complement bit line.

13. The circuit of claim 12 wherein the data latch is coupled to a reference voltage line, further comprising a circuit which disconnects the reference voltage line from the latch when the control signal is activated.

14. A memory circuit, comprising:

a data latch having a true node and a complement node;

a first pass gate coupling the true node to a bit line;

a second pass gate coupling the complement node to a complement bit line; and

a logic circuit generating a logic control signal to simultaneously activate the first and second pass gates to short the true and complement nodes to the bit line and complement bit line, respectively, for the purpose of destroying data stored by the latch.

15. The circuit of claim 14 wherein the data latch is coupled to a reference voltage line, further comprising a circuit which grounds the reference voltage line when the logic circuit generates the logic control signal.

16. A memory circuit, comprising:

a data latch having a true node and a complement node;

circuitry responsive to a control signal to short one of the true/complement nodes of the latch to a reference voltage for the purpose of destroying data stored by the latch.

17. The circuit of claim 16 wherein the circuitry comprises an n-channel transistor having its conduction terminals connected between the one of the true/complement nodes and the reference voltage.

18. The circuit of claim 16 wherein the circuitry comprises a p-channel transistor having its conduction terminals connected between the one of the true/complement nodes and the reference voltage.

19. The circuit of claim 16 wherein the data latch is coupled to a reference voltage line, further comprising a circuit which disconnects the reference voltage line from the latch when the control signal is activated.

20. The circuit of claim 16 wherein the memory circuit further includes:

a first pass gate coupling the true node to a bit line;

a second pass gate coupling the complement node to a complement bit line.

21. A memory circuit, comprising:

a data latch having a true node and a complement node; and

circuitry responsive to at least one control signal to short both the true and complement nodes of the latch to at least one reference voltage for the purpose of destroying data stored by the latch.

22. The circuit of claim 21 wherein the circuitry comprises:

a first n-channel transistor having its conduction terminals connected between the true node and the reference voltage; and

a second n-channel transistor having its conduction terminals connected between the complement node and the reference voltage.

23. The circuit of claim 22 wherein the a gate of the first transistor and a gate of the second transistor receive the same control signal.

24. The circuit of claim 22 wherein the a gate of the first transistor and a gate of the second transistor receive the different control signals.

25. The circuit of claim 21 wherein the circuitry comprises:

a first p-channel transistor having its conduction terminals connected between the true node and the reference voltage; and

a second p-channel transistor having its conduction terminals connected between the complement node and the reference voltage.

26. The circuit of claim 25 wherein the a gate of the first transistor and a gate of the second transistor receive the same control signal.

27. The circuit of claim 25 wherein the a gate of the first transistor and a gate of the second transistor receive the different control signals.

28. The circuit of claim 21 wherein the circuitry comprises:

an n-channel transistor having its conduction terminals connected between one of the true/complement nodes and a first reference voltage; and

a p-channel transistor having its conduction terminals connected between the other of the true/complement nodes and a second reference voltage.

29. The circuit of claim 21 wherein the data latch is coupled to a reference voltage line, further comprising a circuit which disconnects the reference voltage line from the latch when the control signal is activated.

30. The circuit of claim 21 wherein the memory circuit further includes:

a first pass gate coupling the true node to a bit line;

a second pass gate coupling the complement node to a complement bit line.

31. A memory circuit, comprising:

a data latch comprising a first side associated with a true node and having a first positive reference voltage input and a second side associated with a complement node and having a second positive reference voltage input; and

circuitry responsive to at least one control signal to selectively couple the first and second positive reference voltage inputs for the first and second sides of the latch, respectively, to a positive/ground voltage supply for the purpose of destroying data stored by the latch.

32. The circuit of claim 31 wherein the circuitry comprises first and second NOT logic gates coupled to receive the at least one control signal and selectively connect the first and second positive reference voltage inputs for the first and second sides of the latch, respectively, to a positive/ground voltage supply in response thereto.

33. The circuit of claim 31 wherein the cross-coupled data latch comprises a first p-channel transistor for the first side and a second p-channel transistor for the second side, a source terminal of the first p-channel transistor comprising the first positive reference voltage input and a source terminal of the second p-channel transistor comprising the second positive reference voltage input.

34. The circuit of claim 31 wherein the memory circuit further includes:

a first pass gate coupling the true node to a bit line;

a second pass gate coupling the complement node to a complement bit line.

35. A memory circuit, comprising:

a memory cell including a data node;

a pass gate coupling the data node of the memory cell to a bit line; and

circuitry responsive to at least one control signal to short the bit line to a reference voltage while the pass gate is activated for the purpose of destroying data stored by the memory cell.

36. The circuit of claim 35 wherein the circuitry comprises a transistor having conduction terminals connecting the bit line to a reference voltage and a gate coupled to receive the at least one control signal.

37. The circuit of claim 35 wherein the circuitry comprises a first transistor having its conduction terminals connecting the bit line to a first reference voltage and a second transistor having its conduction terminals connecting the bit line to a second reference voltage, the first and second transistors each having a gate coupled to receive the at least one control signal.

38. The circuit of claim 35 further including a coupling circuit for selectively shorting the bit line to a word line to share charge therebetween.

39. The circuit of claim 38 further including a pull up device to pull the word line up to a positive reference voltage after charge has been shared between the bit line and word line.